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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/892,746	YAMAUCHI ET AL.
	Examiner	Art Unit
	John B. Vigushin	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *5 and 13-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 1-4 and 6-12 (Group II) in Paper No. 7 is acknowledged.

Claim Objections

2. Claims 6-8 are objected to because of the following informalities:

In Claim 6, line 5: "and" should be deleted.

In Claim 6, line 12: --the electrodes formed on-- should be inserted after "via".

In Claim 7, line 4: "to" should be changed to --on--.

In Claim 7, line 5: "the" (occurring before "lower") should be changed to --a--.

In Claim 7, line 9: "are" should be changed to --being--.

In Claim 8, line 4: "to" should be changed to --on--.

Appropriate correction is required.

Specification

3. The following is a quotation of 37 CFR § 1.71 (a)-(c):

(a) The specification must include a written description of the invention or discovery and of the manner and process of making and using the same, and is required to be in such full, clear, concise, and exact terms as to enable any person skilled in the art or science to which the invention or discovery appertains, or with which it is most nearly connected, to make and use the same.
(b) The specification must set forth the precise invention for which a patent is solicited, in such manner as to distinguish it from other inventions and from what is old. It must describe completely a specific embodiment of the process, machine, manufacture, composition of matter or improvement invented, and must explain the mode of operation or principle whenever applicable. The best mode

contemplated by the inventor of carrying out his invention must be set forth.
(c) In the case of an improvement, the specification must particularly point out the part or parts of the process, machine, manufacture, or composition of matter to which the improvement relates, and the description should be confined to the specific improvement and to such parts as necessarily cooperate with it or as may be necessary to a complete understanding or description of it.

The Specification is objected to under 37 CFR § 1.71 because it fails to provide an adequate written description of the invention. Specifically, throughout the Specification (in particular: p.5, lines 23-24; p.6, lines 2-3; p.7, lines 17-18 and 23-24; p.8, lines 2-3; p.9, line 23 -p.10, line 3; p.10, lines 17-23; p.11, lines 4-11 and 17-22; p.12, lines 4-10 and 15-17; p.13, lines 8-11; p.14, lines 1-2 and 13-14; p.20, lines 6-8; p.22, lines 19-21, p.24, lines 5-9 and p.24, line 24-p.25, line 1) the Applicant recites that the *electronic components include an element and an electronic component* and references *the element(s)* on one or both of the upper and lower surfaces of the substrate. However, there is no teaching that explains what these elements are in general or in particular. Since the recited *element* could be just about anything connected with a circuit substrate (e.g., a trace, a pad, a material element like Cu, a dielectric layer or portion of the substrate, etc.) the term is essentially meaningless without further explanation, especially as it is used to define an "electronic component" (i.e., an electronic component "including an element and an electronic component"). At this juncture of the prosecution, any attempt to clarify the meaning of "an element" as contemplated by the Applicant **will, in all likelihood, introduce new matter**.

Claim Rejections - 35 USC § 112, 1st paragraph

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

I. Throughout the Specification (in particular: p.5, lines 23-24; p.6, lines 2-3; p.7, lines 17-18 and 23-24; p.8, lines 2-3; p.9, line 23 -p.10, line 3; p.10, lines 17-23; p.11, lines 4-11 and 17-22; p.12, lines 4-10 and 15-17; p.13, lines 8-11; p.14, lines 1-2 and 13-14; p.20, lines 6-8; p.22, lines 19-21, p.24, lines 5-9 and p.24, line 24-p.25, line 1) the Applicant recites that the *electronic components include an element and an electronic component* and references *the element(s)* on one or both of the upper and lower surfaces of the substrate. However, there is no teaching that explains what these elements are in general or in particular. Since the recited *element* could be just about anything connected with a circuit substrate (e.g., a trace, a pad, a material element like Cu, a dielectric layer or portion of the substrate, etc.) the term is essentially meaningless without further explanation, especially as it is used to define an "electronic component" (i.e., an electronic component "including an element and an electronic component"). At this juncture of the prosecution, any attempt to clarify the meaning of

"an element" as contemplated by the Applicant **will, in all likelihood, introduce new matter**. Accordingly, **the Examiner recommends the removal of all occurrences of the concept of *element* from the Specification AND in the Claims 1-4 and 6-10** in order to overcome this 35 USC § 112, 1st paragraph rejection.

Claim Rejections - 35 USC § 112, 2nd paragraph

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3, 4, 6 and 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In Claim 3, line 6, Applicant recites "an upper surface side". There is an implied difference between the recited "upper surface" in line 3 and "an upper surface side" in line 6 which makes no structural sense. The rejection may be overcome by changing "an upper surface side" to --the upper surface-- in line 6.

In Claim 4, line 6, Applicant recites "an upper surface side". There is an implied difference between the recited "upper surface" in line 3 and "an upper surface side" in line 6 which makes no structural sense. The rejection may be overcome by changing "an upper surface side" to --the upper surface-- in line 6.

In Claim 6, lines 3-4, Applicant recites "three or more, or two or more types of electronic components." However, the use of the narrower range "three or more" that falls within the broader range of "two or more" renders the claim indefinite (see MPEP §

2173.05(c), section I). The rejection may be overcome by deleting "three or more, or" in line 3.

In Claim 6, lines 6-7, Applicant recites "a lower surface of the lower surface" which renders the claim indefinite. The rejection may be overcome by deleting "of the lower surface" in lines 6-7.

In Claim 7, Applicant recites "the electronic component" in lines 6 and 8-9. However, it is not clear due to antecedent lines 3-5 of the claim, whether there is *only one* electronic component or *a plurality* of electronic components on each of the upper and lower surfaces with electrodes formed on a side surface of the substrate.

In Claim 8, Applicant recites "the electronic component" in lines 6, 8 and 10 However, it is not clear due to antecedent lines 3-5 of the claim, whether there is *only one* electronic component or *a plurality* of electronic components on each of the upper and lower surfaces with electrodes formed on a side surface of the substrate.

Claims 9 and 10 depend from base Claims 7 and 8, respectively, and therefore inherit the defects of the base claims.

Rejections Based On Prior Art

8. The following references were relied upon for the rejections hereinbelow:

Carpenter (US 6,356,455 B1)

Ehman et al. (US 6,021,050)

Sakamoto et al. (US 5,420,553)

Endo (US 3,775,725)

Handforth et al. (US 6,061,241)

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

10. Claims 1, 3 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto et al.

As to Claim 1 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above), Sakamoto et al. discloses: one substrate 1; three or more electronic components (each including a resistor pattern 2 and conductive elements 4A and 4B) formed on substrate 1 and forming an aggregated planar surface on a surface of substrate 1 (Fig. 1; col.2: 50-55).

As to Claim 3 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above), Sakamoto et al. discloses, in Fig. 1: each of the electronic (resistor) components is formed on an upper surface 1a of substrate 1, and electrodes 4A and 4B corresponding thereto are formed on the upper surface 1a and a side surface 1d of substrate 1 so as to be connected to with other electronic (resistor) component on the upper surface 1a.

As to Claim 11, Sakamoto et al. discloses: a substrate 1, inside of which a capacitor is formed (Figs. 2, 3 and 4; col.3: 8-12); an electronic component (resistor 2) formed on an upper surface 1a of substrate 1 (Fig. 1; col.2; 45-46).

11. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter.

As to Claim 1 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above), Carpenter discloses, in Figs. 5 and 6: one substrate 12; three or more electronic components (resistor, capacitor, inductor) including an element (copper; col.2: 22-24) formed on substrate 12 and forming an aggregated planar surface on a lower surface of substrate 12.

As to Claim 2 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above), Carpenter discloses, in Figs. 5 and 6: one substrate; two or more types of electronic components (resistor, capacitor, inductor) including an element (copper; col.2: 22-24) formed on substrate 12 and forming an aggregated planar surface on a surface of substrate 12 (on the upper surface, the capacitor and the inductor form an aggregated planar surface; on the lower surface, the resistor, capacitor and inductor form an aggregated planar surface).

12. Claims 1, 2 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ehman et al.

As to Claim 1 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above), Ehman et al. discloses, in Figs. 1 and 2, one substrate 10, or alternatively, individual board layer 12; three or more electronic components

(resistors 26; col.2: 63-66) including an element (conductor 30; col.3: 21-26 and col.4: 1-2), formed on the one substrate (10 or 12), forming an aggregated planar surface on a surface of the substrate (Figs. 1 and 2).

As to Claim 2 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above), Ehman et al. discloses, in Figs. 1 and 2, one substrate 10, or alternatively, individual board layer 12; two or more *types* (as defined in Applicant's Specification: p.19, lines 19-23) of electronic components (i.e., resistors 26 of *different resistor values*; col.3: 12-14, 39-41 and 59-67) including an element (conductor 30; col.3: 21-26 and col.4: 1-2), formed on the one substrate (10 or 12), forming an aggregated planar surface on a surface of the substrate (Figs. 1 and 2).

As to Claim 11, Ehman et al. discloses a substrate 10, inside of which a capacitor 42 is formed (col.4: 32-38); an electronic component (resistor 26) formed on an upper surface of the substrate (Figs. 1 and 2; col.3: 12-14).

13. Claims 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Handforth et al.

As to Claim 7 (as best understood by the Examiner in view of the 35 USC § 112, 1st and 2nd paragraph rejections, above), Handforth et al. discloses: one substrate 200; a plurality of electronic components including an element (trim links 210 for the printed resistors 228, 230 on upper surface 206 of substrate 204, and bonding pads and leads on the discrete components mounted to lower surface 205 of substrate 204) distributed on the upper surface 206 and the lower surface 205 of the one substrate 204; electrodes 208 of the upper surface electronic component (say, printed resistor 228)

being formed on a side surface of substrate 204 (Fig. 3), and with the electrodes of the electronic component formed on the lower surface 205 formed on the lower surface of the substrate (for mounting the components on the lower surface 205; Fig. 4).

As to Claim 9, Handforth et al. further discloses a current limiting circuit, not shown, on the lower surface 205 of substrate 204 which includes a FET 24 and a loop resistance (Fig. 4; col.6: 64-col.7: 4). Consequently, the electronic components formed on the upper and lower surfaces 206 and 205, respectively, of substrate 204 are resistors (printed resistor 228 on the upper surface 206, shown in Figs. 2 and 3, and the above-mentioned current limiting loop resistance on the lower surface 205).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.

15. Claims 2, 4 and 6 (as best understood by the Examiner in view of the 35 USC § 112, 1st paragraph rejection, above) are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Sakamoto et al.

A1) As to Claim 2 (rejection under 35 USC § 102(b)):

Sakamoto et al. disclose: one substrate 1; two or more types (resistors) of electronic components (each including a resistor pattern 2 and conductive elements 4A

and 4B) formed on substrate 1 and forming an aggregated planar surface on a surface of substrate 1 (Fig. 1; col.2: 50-55).

A2) As to Claim 2 (rejection under 35 USC § 103(a)):

I. Sakamoto et al. disclose: one substrate 1; two or more types (resistors) of electronic components (each including a resistor pattern 2 and conductive elements 4A and 4B) formed on substrate 1 and forming an aggregated planar surface on a surface of substrate 1.

II. The language of Claim 2 does not require that the types of electronic components (resistors) be *different* types. However, even if the types of electronic components were specified in the claim language as *different* types of electronic components, then, in accordance with the definition of different types of components provided by the Applicant in the Specification, p.19, lines 19-23, Sakamoto et al. still reads on the claim because Sakamoto et al. further teaches that the resistor patterns 2 can be of various widths and shape (col.3: 26-33; col.4: 53-68) and it would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to modify at least some of the resistors in the RC filter of Sakamoto et al. to have individual values that are different from one another by fabricating the widths and/or shapes of the resistors accordingly, in order to obtain an RC filter having the particular equivalent R and C values required for the application.

B) As to Claim 4 (which depends from Claim 2), Sakamoto et al. further discloses, in Fig. 1: each of the electronic (resistor) components is formed on an upper surface 1a of substrate 1, and electrodes 4A and 4B corresponding thereto are formed

on the upper surface 1a and a side surface 1d of substrate 1 so as to be connected to with other electronic (resistor) component on the upper surface 1a.

C1) As to Claim 6 (rejection under 35 USC § 102(b)):

Sakamoto et al. discloses: a substrate 1; two or more types (resistors) of electronic components (each including a resistor pattern 2 connected to the conductive elements of electrodes 4A and 4B) formed on upper surface 1a of substrate 1, with electrodes 4A and 4B corresponding thereto being formed at least on a lower surface (called the "back plane" by Sakamoto et al.) and a side surface (1d and 1e) of substrate 1 (Figs. 1 and 2; col.2: 52-57) so as to be connected to another element (signal line) on the lower surface ("back plane") thereof (col.4: 46-52); the electrodes 4A and 4B provided on the lower surface of the substrate are connected to the electronic components (resistors) on the upper surface of substrate 1 via the electrodes formed on the side surface of substrate 1 (Fig. 1; col.2: 55-57).

C2) As to Claim 6 (rejection under 35 USC § 103(a)):

I. Sakamoto et al. disclose: two or more types (resistors) of electronic components (each including a resistor pattern 2 connected to the conductive elements of electrodes 4A and 4B) formed on the upper surface 1a of substrate 1, as indicated in the paragraph immediately above.

II. The language of Claim 6 does not require that the types of electronic components (resistors) be *different* types. However, even if the types of electronic components were specified in the claim language as *different* types of electronic components, then, in accordance with the definition of *different types* of components

provided by the Applicant in the Specification, p.19, lines 19-23, Sakamoto et al. still reads on the claim because Sakamoto et al. further teaches that the resistor patterns 2 can be of various widths and shape (col.3: 26-33; col.4: 53-68) and it would therefore have been obvious to one of ordinary skill in the art at the time the invention was made to modify at least some of the resistors in the RC filter of Sakamoto et al. to have individual values that are different from one another by fabricating the widths and/or shapes of the resistors accordingly, in order to obtain an RC filter having the particular equivalent R and C values required for the application.

16. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo.

I. Endo discloses: one substrate 1; two or more resistors 8 formed on substrate 1 and set to resistance values different from each other (col.3: 50-col.4: 3; col.4: 23-32; Figs. 3, 4 and 5).

II. The limitation "set in advance" (line 4) and "by trimming" (line 5) are process limitations in a product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985). (Incidentally, Endo discloses setting the resistance values in advance--i.e., before use in an application--by trimming (col.4: 23-32).

III. A "target connecting circuit" is not positively claimed as a structural element of the product, and the substrate 1 with the differently-valued resistors 8 is certainly

capable of being used on any "target connecting circuit" which requires that the substrate have those resistance values. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus form a prior art apparatus (in this case, substrate 1 with resistors 8, of Endo et al.) satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

17. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ehman et al.

I. Ehman et al. discloses one substrate 10 or, alternatively, individual board layer 12, which is also "one substrate;" two or more resistors 26 formed on the one substrate, and set to resistance values different from each other (Figs. 1, 2 and 3; col.3: 12-14, 39-41 and 59-67).

II. The limitation "set in advance" (line 4) and "by trimming" (line 5) are process limitations in a product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985). (Incidentally, Ehman et al. discloses setting the resistance values in advance--i.e., before use in an application--by trimming (Figs. 1, 2 and 3; col.3: 12-14, 39-43 and 59-67; col.4: 24-31).

III. A "target connecting circuit" is not positively claimed as a structural element of the product, and the substrate 1 with the differently-valued resistors 8 is certainly *capable* of being used on any "target connecting circuit" which requires that the substrate have those resistance values. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus form a prior art apparatus (in this case, the substrate with resistors 26, of Ehman et al.) satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

Allowable Subject Matter

18. Claims 8 and 10 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

19. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 8 and 10, patentability resides in **the combination of**: *the electronic components distributed on an upper surface and a lower surface of the one substrate* **and** *the electrodes of the lower surface electronic component formed on a side surface of the substrate having no electrode of the upper surface electronic component*, in further combination with the other limitations of base Claim 8.

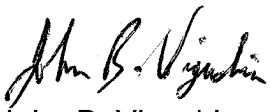
20. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Examiner
Art Unit 2827

jbv
December 30, 2002